ABSTRACT

A CMOS semiconductor device and a method of manufacturing the same in which the gate induced drain leakage (GIDL) effect is reduced. In the semiconductor device of this invention, high concentration source/drain regions of a PMOS transistor are formed away from the gate pattern sidewall spacers. This is accomplished by using as an implant mask a dielectric film formed on an entire surface of a semiconductor substrate, where the semiconductor substrate includes a PMOS transistor region in an n-well, a low concentration source/drain regions of a PMOS transistor formed by using a gate pattern as an implant mask, the PMOS transistor gate pattern sidewall spacers, and an NMOS transistor region in a p-well with the NMOS transistor having both a low concentration and a high concentration source/drain regions.